

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,908,798 B1
APPLICATION NO. : 10/625068
DATED : June 21, 2005
INVENTOR(S) : Arup Bhattacharyya

Page 1 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page #56

In the References Cited:

Col. 2, line 14 -

Replace "Kim, C.H. et al., "A New High -Performance Poly3-Si TFT"
With --Kim, C.H. et al, "A New High -Performance Poly-Si TFT--

In the Specification:

Col. 2, line 44 -

Replace "“High Performance Sub -100 nm Si TFT by Pattem-"
With -- "High Performance Sub- 100 nm Si TFT by Pattern---

Col. 2, line 54 -

Replace "islands for device channel regions. Nickelinduced-lateral"
With --islands for device channel regions. Nickel-induced-lateral---

Col. 3, line 22 -

Replace "Digest, 2002, 00. 98-99; and Huang, L. J. et al.,"
With --Digest, 2002, pp. 98-99; and Huang, L. J. et al.,--

Col. 4, line 20 -

Replace "FIG. 2 is a view of the FIG. 1 wafer shown at a processing"
With --FIG. 2 is a view of the FIG. 1 fragment shown at a processing--

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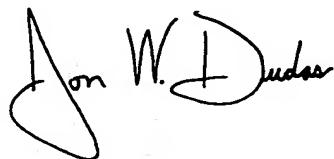
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 10, line 66 -

Replace "similar numbering will be used as in used above In"
With --similar numbering will be used as is used above in--

Signed and Sealed this

Twenty-second Day of August, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office